ABSTRACT OF THE DISCLOSURE

Data bits are prefetched from memory cells in parallel and are read out serially. The memory includes multiple stages (1710) of latches through which the parallel data is transferred before being read out serially. The multiple stages provide suitable delays to satisfy variable latency requirements (e.g. CAS latency in DDR2). The first bit for the serial output bypasses the last stage (1710.M). In some embodiments, the control signals controlling the stages other than the last stage in their providing the first data bit to the memory output are not functions of the control signals controlling the last stage providing the subsequent data bits to the memory output.